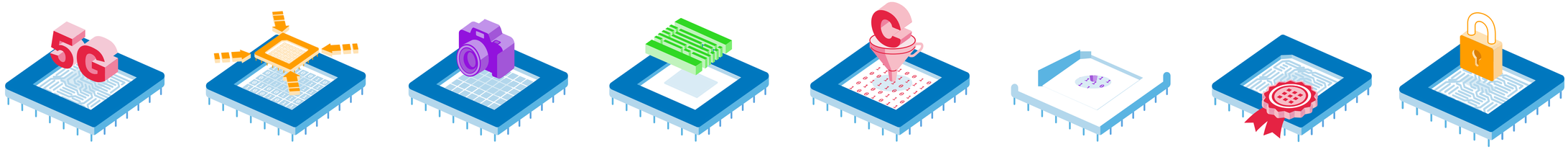
SecureFoundry

Devices that Defend Themselves



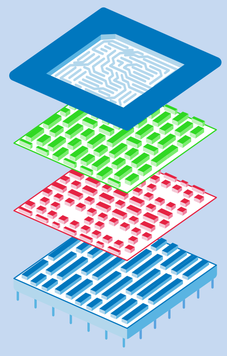
Introducing SecureFoundry

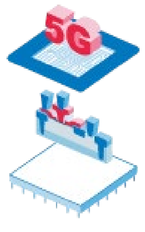
By breaking the mold for e-beam lithography, SecureFoundry introduces the unique benefits of e-beam direct-write to regular semiconductor manufacturing. For decades e-beam systems have been the laboratories' beloved workhorses, due to their high resolution and for the flexibility that comes with not having to create costly masks. Today however, by their single-beam nature, these traditional systems can't scale up to series production: it may take days to expose a fully covered 300 mm wafer at nodes below 90 nm. By deploying up to 650,000 parallel beamlets, it takes only minutes to do the same with SecureFoundry technology. Even at 28 nm. Even at full density.

The SecureFoundry FLX series revolutionizes the use of e-beam lithography: on the one hand it is a perfect companion when researching device characteristics, prototyping new applications and doing specialized low volume applications. On the other hand it is a scalable manufacturing method, an enabler to step up to volume production. Producing thousands of wafers per month with fully customized e-beam layers in mix-and-match operation with optical lithography is now a viable solution.

SecureFoundry applications

High-resolution patterning without a mask enables a broad spectrum of new applications in 200 mm and 300 mm production lines. From making each chip on a wafer truly unique to making wafer-sized MEMS devices. From bringing sub-100 nm resolution into 200 mm fabs to introducing full-2D patterning at advanced nodes.





RF AND 5G

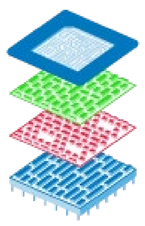
Most mixed-signal devices are made in 200 mm lines where analog performance is uncompromised. However, advanced imaging beyond 90 nm is expensive and unwieldy at 200 mm, imposing a limit on the switching speed of the most critical bipolar devices, such as SiGe transistors.

IOT SECURITY

In a world increasingly connected to the Internet new levels of security are needed to protect our privacy and infrastructure. Connected device functions in the Internet of Things (IoT) must be protected against a growing list of external threats.

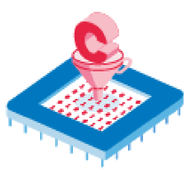
PHOTONICS

If there is one thing that doesn't go well with photonics circuits it is right corners. The FLX can print any feature without design rule restrictions: circles, non-orthogonal shapes, lines and curves. At any width, any spacing and in any orientation, stretched over large areas.



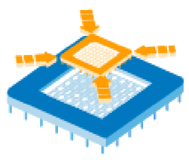
MASK COST REDUCTION

In 300 mm foundries the vast majority of IC designs need fewer than 1,000 wafers. At 40/45 nm nodes and below, soaring mask costs claim a significant chunk of the total budget. In a typical 40-piece mask set, just four advanced phase-shift immersion masks account for one third of the set cost.



VIA ROM

Once a logic IC design gains some level of complexity it often includes a microprocessor unit for on-chip housekeeping tasks. Microprocessors need software to run. If you don't want the complexity of an external non-volatile memory, you have the choice between embedded Flash and Via ROM.

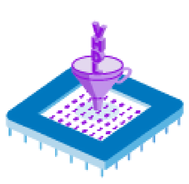


NVRAM CAPACITY INCREASE

If you need a local density increase in an existing design you could look out for a more advanced foundry. However, your design might not need the whole package that a 40/45 nm foundry process comes with. Full node shrink implies new material stacks, different thicknesses and a myriad of design rules.

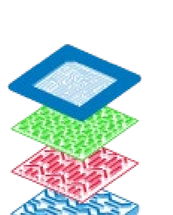
ANTI-COUNTERFEITING AND TRACEABILITY

Miniscule SecureFoundry-made truly unique IC's with short range RF functionality can function as an effective anti-counterfeiting security feature. Not only for medicines and high-value consumer products, such as liquors, perfumes and fashion bags.



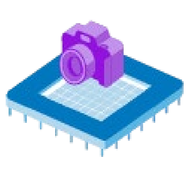
LONG TAIL AND INDUSTRY 4.0

Many foundries are hesitant to accept orders for fewer than 100 wafers. The average IC measures 10 mm^2, therefore 100 wafers yield 500,000 IC's. Many industrial and consumer products don't need that many. In the meantime, Industry 4.0 envisions fast adaptation to increasingly segmented markets.



LAYER REDUCTION IN ADVANCED NODES

Making 28 nm logic devices using 193 nm excimer lasers comes with a trade-off: Rayleigh's limit ($k_1\lambda/NA$) forces IC designs into increasingly regularized and one-dimensional layouts. The indirect cost of low-k_1 manufacturing is a layer count increase and a compromised design for library and custom cells.



LARGE FIELD APPLICATIONS

E-beam patterns are generated on the fly from a computer memory and not from a mask. Such patterns don't confine themselves to a physical field size. With simple memory expansions larger field sizes than 26x33mm^2 become a breeze and eliminate the need for complex stitching schemes.

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